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(71) Applicant: LORAL FAIRCHILD CORPORATION
300 Robbins Lane
Syosset, New York 11791(US)

(72) Inventor: Sayag, Michel
1820 Hackett Avenue
Mountain View, California 94043(US)

(74) Representative: Patentanwälte Grünecker,
Kinkeldey, Stockmair & Partner
Maximilianstrasse 58
D-80538 München (DE)

(54) Electronic color snapshot technique and structure using very high resolution monochrome full frame CCD imagers.

(57) A technique and structure is used for producing high resolution color images using a monochrome area charge-coupled device (CCD) 64 and a sequential color illumination scheme. The monochrome CCD 64 comprises a plurality of semiconductor storage cells 76, the semiconductor storage cells 76 being configured in an array having vertical columns 74 and horizontal rows 79. The entire CCD 64 is exposed to a first color image. The charge packets 82 stored in two adjacent horizontal rows as a result

of the exposure are then shifted into a third horizontal row. The CCD 64 is then exposed to a second color image. The charge packets 82 stored in the first horizontal row as a result of the second exposure are then shifted into the second horizontal row. The CCD 64 is then exposed to a third and final color image. The CCD output is digitized and stored in a frame. The color information of a particular location on the CCD array 64 is derived by utilizing a simple set of equations.

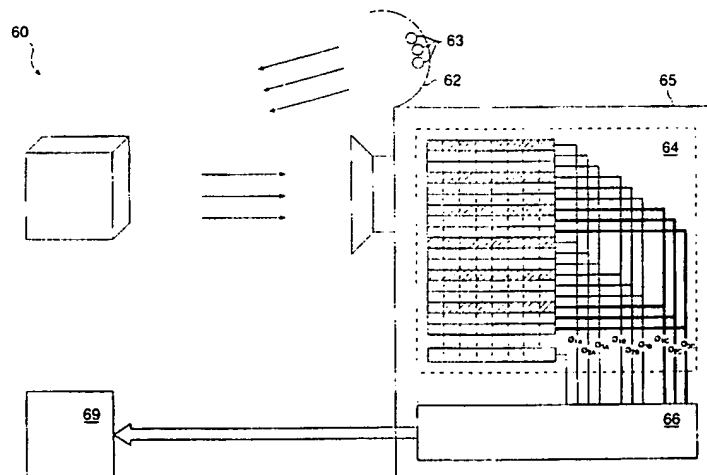


FIG. 6A

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BACKGROUND OF THE INVENTION

This invention relates to a technique and structure for producing very high resolution color images using a monochrome charge-coupled device (CCD) imager and a sequential color illumination scheme.

Conventional schemes for obtaining color electronic snapshots have traditionally employed one of three techniques. The first of these techniques uses white light illumination of a color CCD imager (Fig. 1). A color CCD imager 10 comprises a monochrome CCD imager upon which color sensitive stripes 14, 16, and 18 are deposited resulting in a mosaic of color pixels 12. The stripes are generally photo sensitive to alternating complementary colors such as red, green, and blue.

The second technique uses white light illumination of a color CCD imaging module. As illustrated by Fig. 2, a color CCD imaging module 20 employs three monochrome CCD imagers 22, 24, and 26 placed behind a beam-splitter 28. The beam-splitter separates the incoming radiation 30 into three beams of different spectral bands (typically, red 32, green 34, and blue 36), with each imaging module storing one of the monochrome images. Both of these techniques can be used to obtain snapshots of subject matter with brief exposure time (e.g., moving objects), however the cost is considerable.

A third technique, as shown in Fig. 3, employs a system 40 which uses a monochrome CCD imager with a sequential color illumination scheme. A filter wheel 42 is rotated in front of the imager 44 or the light source 46 so that the imager is exposed to a series of the color images which are then read out sequentially. This technique is less expensive than the previously described techniques, but has limitations in the subject matter for which it can be used. Because the monochrome imager is generally exposed to three color images sequentially, the exposure time for obtaining a complete image is often longer than that required for the other techniques.

This problem is aggravated by the fact that the preferred CCD imager architecture for very high resolution color snapshots is the full frame architecture. The full frame architecture provides the highest pixel density but at the cost of maintaining a storage area. As a result of the fact that there is no storage area, image integration and readout times have to be successive rather than simultaneous as with other architectures used, for example, in video applications. Because of the need to shield the imager during successive image read-outs the total exposure time must include three integration times (one for each color) and two read-out times.

Fig. 4 shows a timing diagram which is representative of a typical exposure time. The top time

line 47 is the integration time line which indicates when the CCD imager is exposed to an image. The middle time line 48 is the read-out time line which indicates when a stored image is being read out. The bottom time line 49 is the total exposure time line which represents the time required to acquire a complete color image.

At t_1 , the imager is exposed to the blue portion of the image (integration time line 47). The image stored during the exposure is then read out beginning at time t_2 (read-out time line 48). After the image is downloaded, the imager is exposed to the red portion of the image at t_3 . The red portion of the image is then downloaded at time t_4 . Finally, at t_5 the imager is exposed to the green portion of the image which is read out at t_6 . Thus, as illustrated on the total exposure time line 49, this imaging scheme requires three exposures and two read-out intervals before a complete color image can be obtained. In addition, the high density of pixels and sequential nature of the downloading of imaging information further increases the total exposure time, often taking as long as five to ten seconds for a complete color image to be stored. The result being that this technique is unsuitable for creating images of moving subject matter.

Fig. 5 shows a simplified representation of a conventional three-phase full frame CCD imager 50 which can be used with any of the above-described techniques. Three gate electrodes 52 of each individual semiconductor storage cell 54 (one such cell shown outlined in bold lines) are controlled by one set of clock signals ϕ_1 , ϕ_2 , and ϕ_3 . Charge which is stored in each row of cells is shifted into a horizontal CCD register 56 from which it can be read out serially through output 58.

In light of the preceding discussion, it is apparent that there exists a need for a full frame, color CCD imager which combines the low cost of sequential color illumination with the speed of costly white light illumination schemes.

SUMMARY OF THE INVENTION

According to the invention, a technique and structure is provided for producing high resolution color images using a monochrome charge-coupled device (CCD) imager and a sequential color illumination scheme. The monochrome CCD imager comprises a plurality of semiconductor storage cells, the semiconductor storage cells being configured in an array having vertical columns and horizontal rows. Each vertical column comprises a CCD register that is isolated from adjacent columns by potential barriers. Each semiconductor storage cell, or pixel, has at least one gate electrode which controls the potential profile of the cell.

The invention uses a plurality of sets of clocks, each of which controls a portion of the horizontal rows of pixels. The gate electrodes of the pixels in a particular horizontal row are all connected to a single set of clocks. The horizontal rows controlled by one set of clocks are separated from others controlled by the same set of clocks by intervening rows which are controlled by other sets of clocks.

The procedure by which an image is stored will be described with reference to an embodiment of the invention in which three sets of clocks are employed, and each pixel has three gate electrodes. This is by no means the only configuration by which the invention may be implemented. To begin the procedure, the entire monochrome CCD imager is exposed to a first color image. The charge packets stored in the first and second sets of horizontal rows as a result of the exposure are then shifted into the third set of horizontal rows of pixels. The entire CCD imager is again exposed to a second color image. The charge packets stored in the first set of horizontal rows are then shifted into the second set of horizontal rows. The CCD imager is then exposed to a third and final color image.

To download the stored image, all of the vertical gate electrodes are clocked and shifted and all of the charge packets stored in each horizontal row are clocked into a horizontal register and then read out sequentially. The CCD imager output is digitized and stored in a frame. The color information of a particular location on the CCD array is derived by utilizing a simple set of equations described below.

Thus, the invention comprises an apparatus and method for producing color images using a monochrome charge-coupled device, the monochrome charge-coupled device comprising a plurality of semiconductor storage cells being controlled by gate electrodes, the semiconductor storage cells being configured in an array comprising vertical columns and horizontal rows. The method comprises the steps of: exposing the monochrome charge-coupled device to a first color portion of an image; moving charge packets stored in a first set of horizontal rows of semiconductor storage cells into a second set of horizontal rows of semiconductor storage cells; repeating said exposing and moving steps where the number of color portions of the image to which the charge-coupled device is exposed exceeds two, the steps to be repeated for each exposure in excess of two; exposing the monochrome charge-coupled device to a final color portion of the image; downloading final charge packets stored in each horizontal row of semiconductor storage cells into a horizontal charge-coupled device register, the horizontal charge-coupled device register storing the final charge packets from one horizontal row of semiconductor storage

cells at a time; serially outputting from the horizontal charge-coupled device register the final charge packets from each horizontal row of semiconductor storage cells; storing digital information corresponding to the final charge packets; and processing the digital information to derive color information corresponding to locations on the monochrome charge-coupled device.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified representation of a representative monolithic charge-coupled device color imager.

Fig. 2 is a simplified representation of a representative charge-coupled device color module.

Fig. 3 is a simplified representation of a monochrome charge-coupled device imager camera system with a sequential color illumination scheme.

Fig. 4 is a timing diagram for a representative monochrome charge-coupled device imager camera system.

Fig. 5 is a simplified representation of a representative three-phase full frame charge-coupled device imager.

Fig. 6a is a block diagram of one embodiment of a photographic imaging system designed in accordance with the invention.

Fig. 6b is a block diagram of a second embodiment of a photographic imaging system designed in accordance with the invention.

Fig. 7 is a simplified representation of a preferred embodiment of a full frame charge-coupled device imager designed in accordance with the invention.

Fig. 8a-l are stylized illustrations of the potential profile of a portion of a vertical CCD column constructed in accordance with a preferred embodiment of the invention at various times during the imaging process.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 6a and 6b are block diagrams of a two preferred embodiments of a photographic imaging system, 60 and 60'. In Fig. 6a, an illumination source 62 illuminates the subject matter 61, and thereby, the photosensitive surface of the CCD imager 64 contained in camera 65. This embodiment of the invention employs three strobe lights 63 to implement the illumination source 62. Each of the strobe lights 63 is equipped with a different color filter. To avoid image distortion such as color shadows, it is generally important to ensure that the three strobe lights 63 illuminate the scene from substantially the same angle. This may be accomplished by placing the strobe lights 63 as close

together as possible, or by using a coaxial beam-splitter arrangement. The use of diffusers may also reduce the potential problem of color shadows.

Another embodiment of the invention, shown in Fig. 6b, employs a "color focal plane" shutter 67 in front of the monochrome CCD imager 64. The "color focal plane" shutter 67 is similar to conventional focal plane shutters. The shutter comprises three aperture slits 68 moving rapidly across the focal plane, thereby filtering the light from the white light illumination source 62'.

The imager 64 is controlled by a microcomputer 66 which manipulates the clock signals ϕ , and which may perform any of the following functions: downloading the stored image; storing the image; processing the image; outputting the image to a display means 69 which may comprise, for example, a color printer or a video monitor; and controlling the strober 62 or shutter 67.

Fig. 7 illustrates a portion of a monochrome CCD imager 64 constructed in accordance with the invention. Each column 74 (separated by potential barriers 72) represents a CCD register comprising a plurality of photosensitive semiconductor storage cells 76 (one such cell is outlined in bold lines). Each cell has three polysilicon gate electrodes 78 by which the cell's potential profile may be controlled using clock signals ϕ . Each horizontal row 79 of cells 76 is controlled by one set of clocks out of three sets of clocks (e.g., Row 1 is controlled by a set of clocks ϕ_{1A} , with $n = 1, 2$, and 3), with each set of clocks controlling every third row as shown. Each set of clock signals is distinct from the other two sets of clock signals.

A preferred architecture for a very high resolution full frame CCD imager is defined as follows:

CCD imager active area size: $2\frac{1}{4}" \times 2\frac{1}{4}"$ (60mm x 60mm) (i.e., compatible with the large negative format of very high resolution photography equipment, such as in cameras made by Hasselblad)

Pixel size: $10\mu\text{m}$ (vertical) x $30\mu\text{m}$ (horizontal)

Pixel count: 6000 (vertical) x 2000 (horizontal)

Horizontal CCD register: 2000 pixels

"Color Pixel" size: $30\mu\text{m} \times 30\mu\text{m}$ (3 monochrome pixels)

"Color Pixel" resolution: 2000 pixels x 2000 pixels

In the preferred embodiment, the entire CCD imager is exposed initially to the blue portion of the image. Blue is the preferred first color exposure because the blue portion of an image has the lowest energy. Figs. 8a through 8i are idealized representations of potential profiles of a portion of one CCD column at various stages during the acquisition of an image. At time t_0 , immediately following the blue exposure, the CCD column is in the state shown in Fig. 8a. The "wells" 82 in which charge packets 84 (designated by cross-hatched

and shaded areas) are deposited by the exposure are potential wells created by bias voltages on the clock lines ϕ . The profile shown in Fig. 8a is created by the following state: ϕ_{1A} , ϕ_{1B} , ϕ_{1C} , ϕ_{2A} , ϕ_{2B} , and ϕ_{2C} are held high, and ϕ_{3A} , ϕ_{3B} , and ϕ_{3C} are held low. At t_1 , the voltage on ϕ_{1A} is brought low while the voltage on ϕ_{3A} is brought high. This alters the potential profile of the CCD column as shown in Fig. 8b. At t_2 , the voltage on ϕ_{1A} is brought high again while the voltage on ϕ_{2A} is brought low. This alters the potential profile of the CCD column as shown in Fig. 8c. At t_3 , the voltage on ϕ_{2A} is brought high again while the voltage on ϕ_{3A} is brought back low. This alters the potential profile of the CCD column as shown in Fig. 8d. At this point, the charge packets 84 are stored, for example, in rows 2, 3, 5, and 6, leaving rows 1 and 4 empty.

At t_4 , the voltage on ϕ_{1B} is brought low while the voltage on ϕ_{3B} is brought high. This alters the potential profile of the CCD column as shown in Fig. 8e. At t_5 , the voltage on ϕ_{1B} is brought back high while the voltage on ϕ_{2B} is brought low. This alters the potential profile of the CCD column as shown in Fig. 8f. Finally, at t_6 , the voltage on ϕ_{2B} is brought back high while the voltage on ϕ_{3B} is brought low again. This alters the potential profile of the CCD column as shown in Fig. 8g. Thus, for example, the entire blue portion of the image is shifted from rows 1 and 2 into row 3, and from rows 4 and 5 into row 6, leaving rows 1, 2, 4 and 5 empty. This shifting of charge packets 84 occurs in a similar manner across the CCD array.

At t_7 , immediately after the CCD imager is exposed to the red portion of the image, the state of the clocks lines is again as follows: ϕ_{1A} , ϕ_{1B} , ϕ_{1C} , ϕ_{2A} , ϕ_{2B} , and ϕ_{2C} are held high, and ϕ_{3A} , ϕ_{3B} , and ϕ_{3C} are held low. The charge packets 84 are distributed as shown in Fig. 8h, with the cross-hatched regions representing charge from the blue exposure, and the shaded regions representing charge from the red exposure. At t_8 , the voltage on ϕ_{3A} is brought high while the voltage on ϕ_{1A} is brought low. This alters the potential profile of the CCD column as shown in Fig. 8i. At t_9 , the voltage on ϕ_{1A} is brought back high while the voltage on ϕ_{2A} is brought low. This alters the potential profile of the CCD column as shown in Fig. 8j. At t_{10} , the voltage on ϕ_{2A} is brought back high while the voltage on ϕ_{3A} is again brought low. This alters the potential profile of the CCD column as shown in Fig. 8k. Thus, the red portion of the image is moved, for example, from row 1 into row 2 and from row 4 into row 5. A portion of the red image remains in rows 3 and 6 undisturbed. Rows 1 and 4 are again left empty.

Finally, the entire imager is exposed to the green portion of the image, a portion of which is

stored in all of the rows at t_{11} (Fig. 81).

If one assumes that the light level on three adjacent rows is approximately the same, the technique described above will result in the following approximate charge distribution in the adjacent pixels. Rows 3, 6, and 9 will contain the entire blue portion of the image, 1/3 of the red portion, and 1/3 of the green portion. Rows 2, 5, and 8 will contain 2/3 of the red portion, and 1/3 of the green portion. Rows 1, 4, and 7 will contain only 1/3 of the green portion of the image.

In order for the assumption described above to be valid, the optics of the CCD imager is, in some embodiments, designed to ensure that the imager is incapable of resolving images below a certain critical level. To achieve this result, each pixel is equipped with a plate of birefringent material, such as calcite, which acts to "smear" the incident image, thus acting as a resolution limit.

After exposure to the desired image is complete, the stored charge is downloaded in the following manner. All of the gate electrodes are clocked in a repeating three-phase sequence (the gate electrodes in each horizontal row being clocked simultaneously) and the charge packets stored in each horizontal row are shifted down the array and placed in a horizontal CCD register. Each row is then clocked out sequentially. The output is then digitized and stored in a frame memory for later display or printing.

When deriving an image from the frame memory for displaying or printing, the red, green, and blue color information of a particular "color pixel" is derived. In a preferred embodiment, a color pixel in a derived image corresponds to three vertically adjacent monochrome pixels in the CCD imager. Thus, for example, a color pixel would comprise 3 monochrome pixels from Rows A, B, and C, where Rows A, B, and C are derived according to the following discussion.

The pixels of rows 1, 4, and 7 contain only green information. Therefore, because of the simplifying approximation outlined above, the full value for the green rows can be obtained by multiplying the values stored in rows 1, 4, and 7 by three. This may be represented by the following equations:

$$\begin{aligned}\text{Row A} &= \text{Row 1} \cdot 3 \\ \text{Row D} &= \text{Row 4} \cdot 3 \\ \text{Row G} &= \text{Row 7} \cdot 3\end{aligned}$$

Rows A, D, and G corresponding to rows of green pixels in the displayed or printed image.

The pixels of rows 2, 5, and 8 contain both red and green information. Again because of the simplifying assumption, the full value of the red rows can be obtained by subtracting the value stored for rows 1, 4, and 7 from the value stored in rows 2, 5,

and 8 and multiplying the result by 3/2. This is represented by the following equations:

$$\begin{aligned}\text{Row B} &= 3/2 \cdot (\text{Row 2} - \text{Row 1}) \\ \text{Row E} &= 3/2 \cdot (\text{Row 5} - \text{Row 4}) \\ \text{Row H} &= 3/2 \cdot (\text{Row 8} - \text{Row 7})\end{aligned}$$

Rows B, E, and H corresponding to rows of red pixels in the displayed or printed image.

Finally, the full value of the blue rows can be obtained by adding the value of rows 1, 4, and 7 to the value of rows 2, 5, and 8, dividing the resulting value by 2 and subtracting that number from the value stored in rows 3, 6, and 9. This is represented by the following equations:

$$\begin{aligned}\text{Row C} &= \text{Row 3} - 1/2 (\text{Row 1} + \text{Row 2}) \\ \text{Row F} &= \text{Row 6} - 1/2 (\text{Row 4} + \text{Row 5}) \\ \text{Row I} &= \text{Row 9} - 1/2 (\text{Row 7} + \text{Row 8})\end{aligned}$$

Rows C, F, and I corresponding to rows of blue pixels in the displayed or printed image.

An alternate means of processing the stored information to derive the rows of blue pixels is represented by the following equations:

$$\begin{aligned}\text{Row C} &= \text{Row 3} - 1/4 (\text{Row 1} + \text{Row 2} + \text{Row 4} \\ &\quad + \text{Row 5}) \\ \text{Row F} &= \text{Row 6} - 1/4 (\text{Row 4} + \text{Row 5} + \text{Row 7} \\ &\quad + \text{Row 8}) \\ \text{Row I} &= \text{Row 9} - 1/4 (\text{Row 7} + \text{Row 8} + \text{Row 10} \\ &\quad + \text{Row 11})\end{aligned}$$

This alternate processing method more accurately derives the blue portion of an image when the simplifying assumption outlined above lacks validity as may sometimes be the case. These equations, in effect, average the values stored in the rows above and below the row to be derived rather than only allowing the rows above the row to be derived to contribute to the final image. In still further embodiments, nearest or near neighbor analysis will further enhance the accuracy of the image.

While the invention has been particularly shown and described with reference to specific embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in the form and details may be made therein without departing from the spirit or scope of the invention. Specifically, while the embodiment described above employs a three-phase CCD imager, it will be evident to those skilled in the art that the invention may be implemented using a number of different schemes. For example, if permanent barriers are implanted between adjacent cells, it is possible to achieve the desired shifting functions with fewer than three gate electrodes on each cell. Further, the number of sets of clock

signals may vary with the number of colors desired to be stored. Consequently, the scope of the invention should be determined solely with respect to the following claims.

Claims

1. A method for producing color images using a monochrome charge-coupled device, the monochrome charge-coupled device comprising a plurality of semiconductor storage cells being controlled by gate electrodes, the semiconductor storage cells being configured in an array comprising vertical columns and horizontal rows, the method comprising the steps of:
 - exposing the monochrome charge-coupled device to a first color portion of an image;
 - moving charge packets stored in a first set of horizontal rows of semiconductor storage cells into a second set of horizontal rows of semiconductor storage cells;
 - repeating said exposing and moving steps where the number of color portions of the image to which the charge-coupled device is exposed exceeds two, the exposing and moving steps to be repeated for each exposure in excess of two;
 - exposing the monochrome charge-coupled device to a final color portion of the image;
 - downloading final charge packets stored in each horizontal row of semiconductor storage cells into a horizontal charge-coupled device register, the horizontal charge-coupled device register storing the final charge packets from one horizontal row of semiconductor storage cells at a time;
 - serially outputting from the horizontal charge-coupled device register the final charge packets from each horizontal row of semiconductor storage cells;
 - storing digital information corresponding to the final charge packets; and
 - processing the digital information to derive color pixel information corresponding to locations on the monochrome charge-coupled device.
2. A method as described in claim 1 wherein the exposing steps are accomplished by means of strobe lights, each of the strobe lights being equipped with a color filter.
3. A method as described in claim 1 wherein the exposing steps are accomplished by means of white light illumination of a shutter interposed between the white light source and the array of semiconductor storage cells, the shutter having a plurality of apertures with color filters, the apertures moving sequentially across the array of semiconductor storage cells.
4. A method as described in claim 1 wherein the moving steps comprise selectively applying clock signals to the gate electrodes to move charge packets from a first horizontal row of semiconductor storage cells to a second horizontal row of semiconductor storage cells, the second row of semiconductor storage cells being below the first row of semiconductor storage cells.
5. A method as described in claim 1 wherein the downloading step comprises applying clock signals to the gate electrodes in a repeating multi-phase sequence to shift the final charge packets stored in the semiconductor storage cells into the horizontal charge-coupled device register.
6. A method for producing color images using a monochrome charge-coupled device, the monochrome charge-coupled device comprising a plurality of semiconductor storage cells being controlled by gate electrodes, the semiconductor storage cells being configured in an array comprising vertical columns and horizontal rows, the method comprising the steps of:
 - exposing the monochrome charge-coupled device to a first portion of an image, the first portion of the image being of a first color;
 - moving first charge packets stored in a first set of horizontal rows of semiconductor storage cells into a second set of horizontal rows of semiconductor storage cells;
 - exposing the monochrome charge-coupled device to a second portion of the image, the second portion of the image being of a second color;
 - moving second charge packets stored in a third set of horizontal rows of semiconductor storage cells into a fourth set of horizontal rows of semiconductor storage cells;
 - exposing the monochrome charge-coupled device to a third portion of the image, the third portion of the image being of a third color;
 - downloading third charge packets stored in each horizontal row of semiconductor storage cells into a horizontal charge-coupled device register, the horizontal charge-coupled device register storing the third charge packets from one horizontal row of semiconductor storage cells at a time;
 - serially outputting the third charge packets from the horizontal charge-coupled device register;
 - storing digital information corresponding to

the third charge packets; and

processing the digital information to derive color pixel information corresponding to locations on the monochrome charge-coupled device.

7. A method as described in claim 6 wherein the first, second, and third colors comprise complementary colors.

8. A method as described in claim 6 wherein the exposing steps are accomplished by means of three strobe lights, each of the strobe lights being equipped with a color filter.

9. A method as described in claim 6 wherein the exposing steps are accomplished by means of white light illumination of a shutter interposed between the white light source and the array of semiconductor storage cells, the shutter having three apertures with color filters, the apertures moving sequentially across the array of semiconductor storage cells.

10. A method as described in claim 6 wherein the moving steps comprise selectively applying clock signals to the gate electrodes to move the first and second charge packets from a first horizontal row of semiconductor storage cells to a second horizontal row of semiconductor storage cells, the second row of semiconductor storage cells being below the first row of semiconductor storage cells.

11. A method as described in claim 6 wherein the downloading step comprises applying clock signals to the gate electrodes in a repeating three-phase sequence to shift the third charge packets stored in the semiconductor storage cells into the horizontal charge-coupled device register.

12. A monochrome charge-coupled device for producing color images using a sequential color illumination scheme, the monochrome charge-coupled device comprising:

a plurality of semiconductor storage cells, the semiconductor storage cells being configured in an array having vertical columns and horizontal rows, the vertical columns being separated by potential barriers;

a plurality of gate electrodes, each semiconductor storage cell being controlled by at least one gate electrode, the gate electrodes controlling potential profiles of the semiconductor storage cells; and

a plurality of sets of clock lines, each set of clock lines conducting a distinct set of clock

signals, the number of clock lines in each set of clock lines being equal to the number of gate electrodes controlling each semiconductor storage cell, each set of clock lines being connected to the gate electrodes of the semiconductor storage cells in a particular horizontal row of semiconductor storage cells, the gate electrodes of adjacent horizontal rows being connected to different sets of clock lines.

13. A monochrome charge-coupled device as described in claim 12 wherein the number of sets of clock lines is three, a first set of clock lines being connected to the gate electrodes controlling the semiconductor storage cells in a first set of horizontal rows, the first set of horizontal rows comprising the top horizontal row of semiconductor storage cells and each third horizontal row of semiconductor storage cells below the top horizontal row, a second set of clock lines being connected to the gate electrodes controlling the semiconductor storage cells in a second set of horizontal rows, the second set of horizontal rows comprising horizontal rows immediately below a horizontal row from the first set of horizontal rows, and a third set of clock lines being connected to the gate electrodes controlling the semiconductor storage cells in a third set of horizontal rows, the third set of horizontal rows comprising horizontal rows not from the first and second sets of horizontal rows.

14. A monochrome charge-coupled device as described in claim 12 wherein the number of gate electrodes controlling each semiconductor storage cell is three.

15. A monochrome charge-coupled device as described in claim 12 further comprising a birefringent material, each semiconductor storage cell being covered by the birefringent material.

16. A monochrome charge-coupled device as described in claim 15 wherein the birefringent material comprises calcite.

17. A monochrome charge-coupled device as described in claim 12 wherein each vertical column of semiconductor storage cells comprises 6000 pixels, and each horizontal column of semiconductor storage cells comprises 2000 pixels, each pixel having a horizontally measured width and a vertically measured height, the width of each pixel being 30 μm , and the height of each pixel being 10 μm .

18. A monochrome charge-coupled device for producing color images using a sequential color illumination scheme, the monochrome charge-coupled device comprising:

a plurality of photosensitive semiconductor storage cells, the semiconductor storage cells being configured in an array having vertical columns and horizontal rows, the vertical columns being separated by potential barriers;

a plurality of gate electrodes, each semiconductor storage cell comprising three gate electrodes, the gate electrodes controlling potential profiles of the semiconductor storage cells;

a first set of clock lines, the first set of clock lines conducting a first set of clock signals, and being connected to the gate electrodes of the semiconductor storage cells in a first set of horizontal rows, the first set of horizontal rows comprising the top horizontal row of semiconductor storage cells and each third horizontal row of semiconductor storage cells below the top horizontal row;

a second set of clock lines, the second set of clock lines conducting a second set of clock signals, and being connected to the gate electrodes of the semiconductor storage cells in a second set of horizontal rows, the second set of horizontal rows comprising horizontal rows immediately below a horizontal row from the first set of horizontal rows;

a third set of clock lines, the third set of clock lines conducting a third set of clock signals, and being connected to the gate electrodes of the semiconductor storage cells in a third set of horizontal rows, the third set of horizontal rows comprising horizontal rows not from the first and second sets of horizontal rows; and

a birefringent material, each semiconductor storage cell being covered by the birefringent material.

19. A camera for producing color images comprising:

a microcomputer for controlling the operation of the camera;

a monochrome charge-coupled device further comprising:

a plurality of photosensitive semiconductor storage cells, the semiconductor storage cells being configured in an array having vertical columns and horizontal rows, the vertical columns being separated by potential barriers;

a plurality of gate electrodes, each semiconductor storage cell comprising three gate electrodes, the gate electrodes controlling potential profiles of the semiconductor storage

cells;

a first set of clock lines, the first set of clock lines conducting a first set of clock signals, and being connected to the gate electrodes of the semiconductor storage cells in a first set of horizontal rows, the first set of horizontal rows comprising the top horizontal row of semiconductor storage cells and each third horizontal row of semiconductor storage cells below the top horizontal row;

a second set of clock lines, the second set of clock lines conducting a second set of clock signals, and being connected to the gate electrodes of the semiconductor storage cells in a second set of horizontal rows, the second set of horizontal rows comprising horizontal rows immediately below a horizontal row from the first set of horizontal rows;

a third set of clock lines, the third set of clock lines conducting a third set of clock signals, and being connected to the gate electrodes of the semiconductor storage cells in a third set of horizontal rows, the third set of horizontal rows comprising horizontal rows not from the first and second sets of horizontal rows; and

an illumination means;

an exposure means for sequentially exposing the charge-coupled device to a plurality of color portions of an image; and

a horizontal charge-coupled device register for downloading stored image information from the charge-coupled device.

20. A camera as described in claim 19 wherein the illumination means comprises three strobe lights, each of the strobe lights being equipped with a color filter.

21. A camera as described in claim 19 wherein the illumination means comprises a white light source.

22. A camera as described in claim 21 wherein the exposure means comprises a shutter interposed between the white light source and the array of semiconductor storage cells, the shutter having three apertures with color filters, the apertures moving sequentially across the array of semiconductor storage cells.

23. A camera as described in claim 19 further comprising a birefringent material, each semiconductor storage cell being covered by the birefringent material.

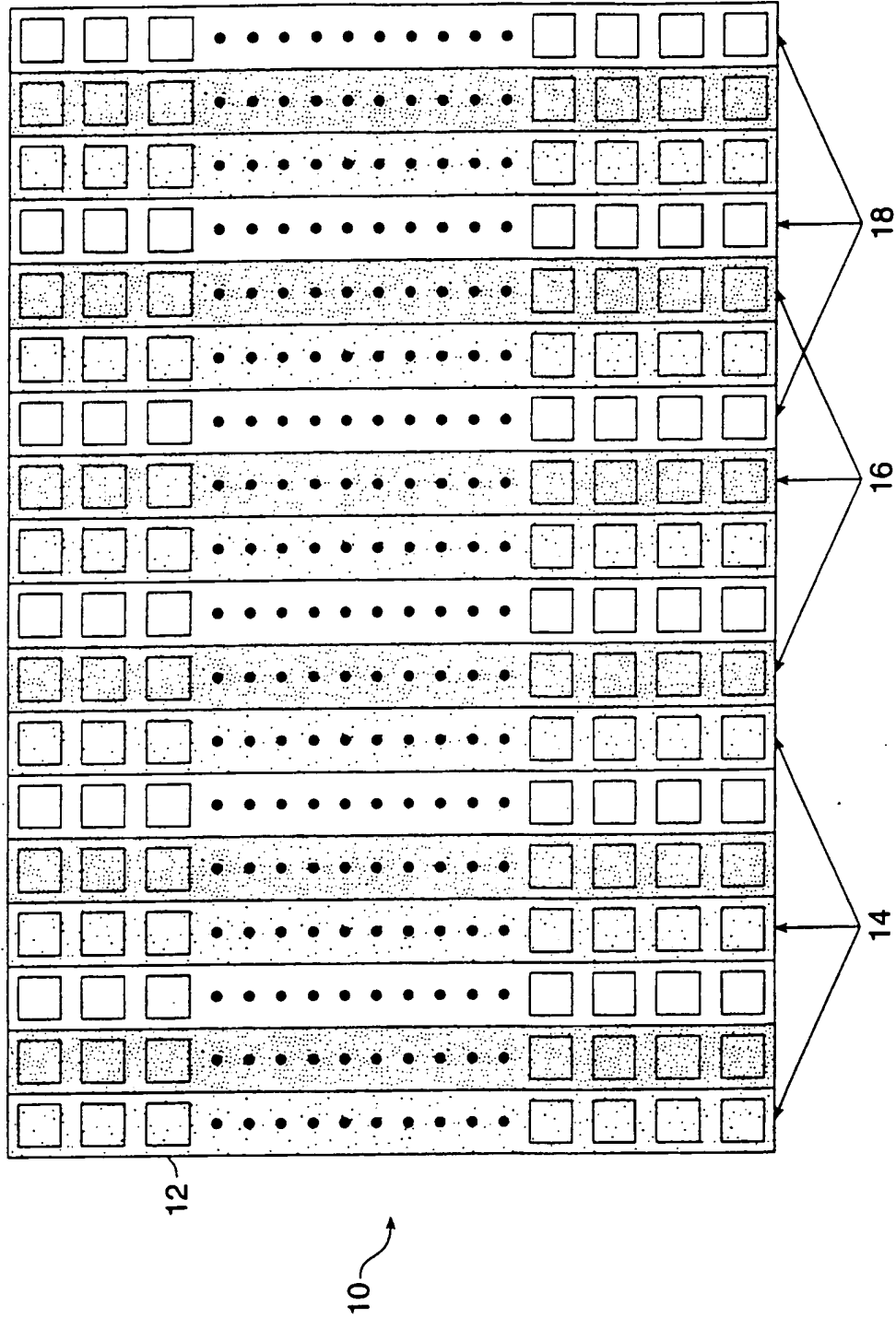


FIG. 1
(PRIOR ART)

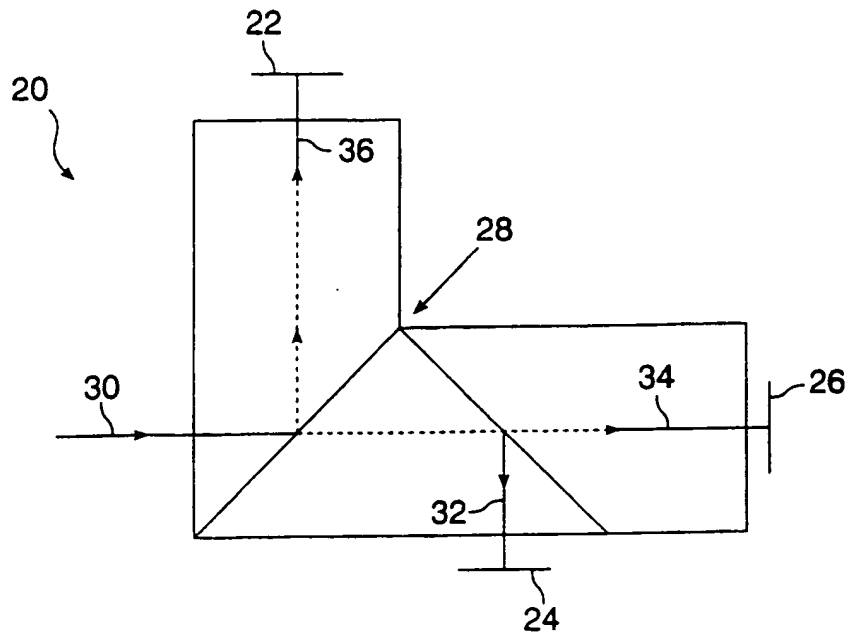


FIG. 2
(PRIOR ART)

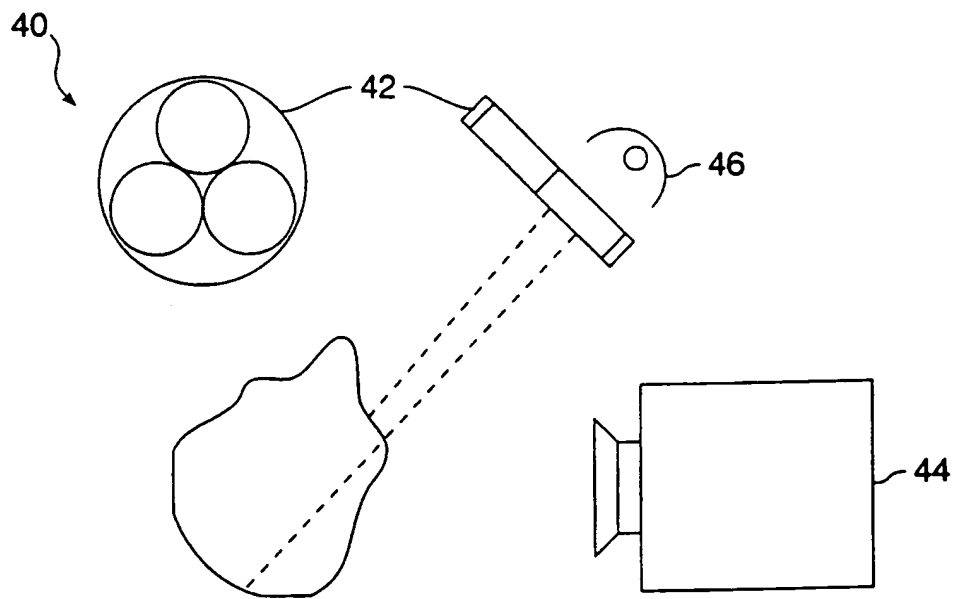


FIG. 3
(PRIOR ART)

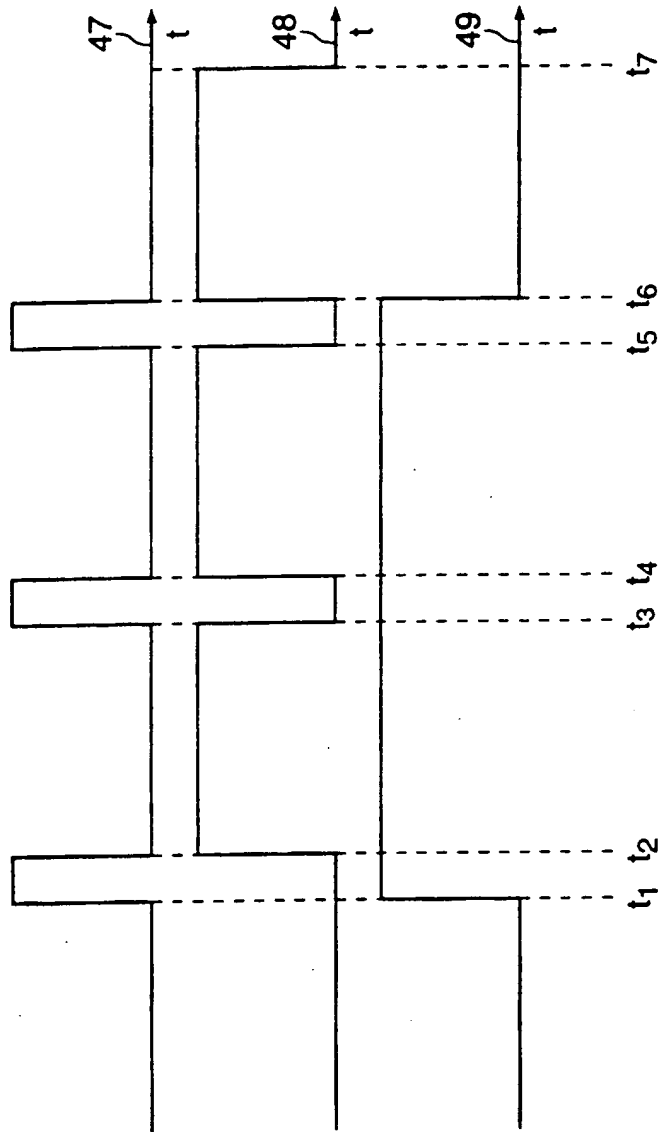


FIG. 4
(PRIOR ART)

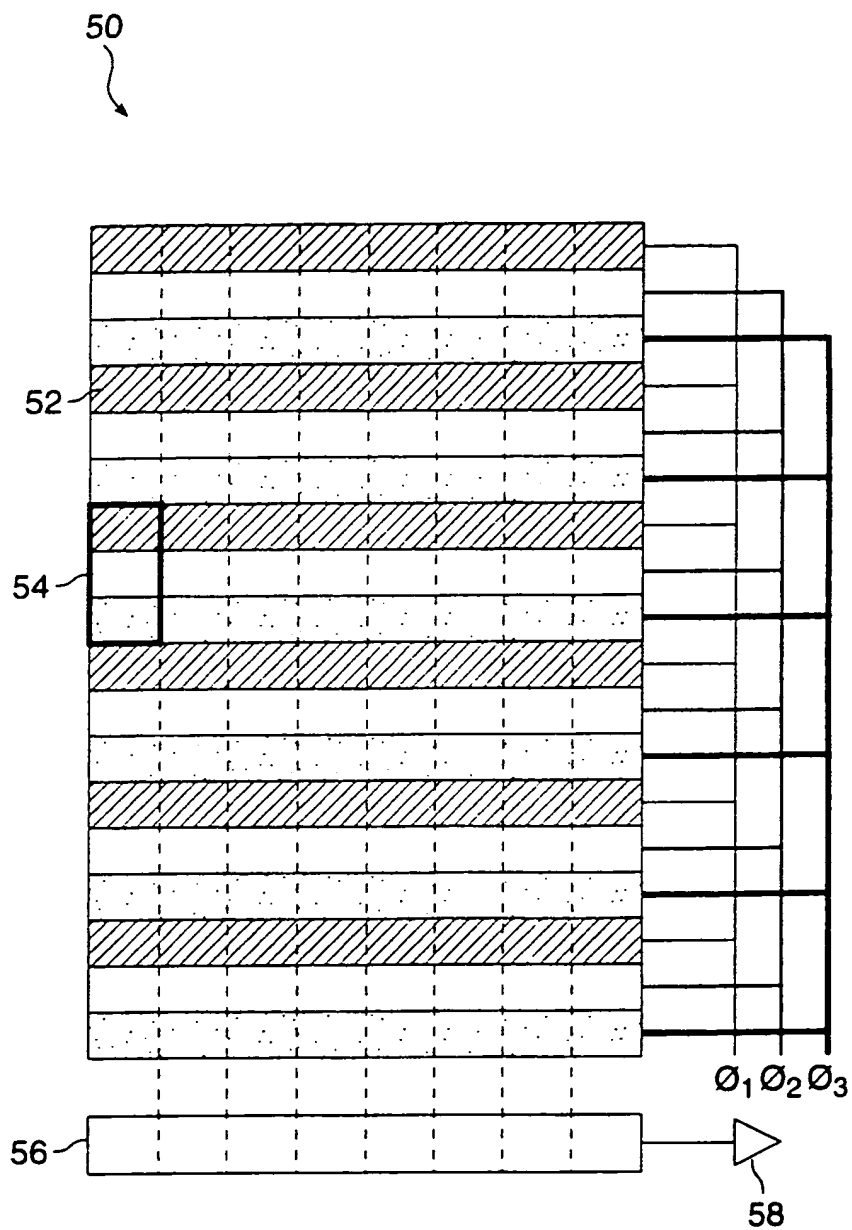


FIG. 5
(PRIOR ART)

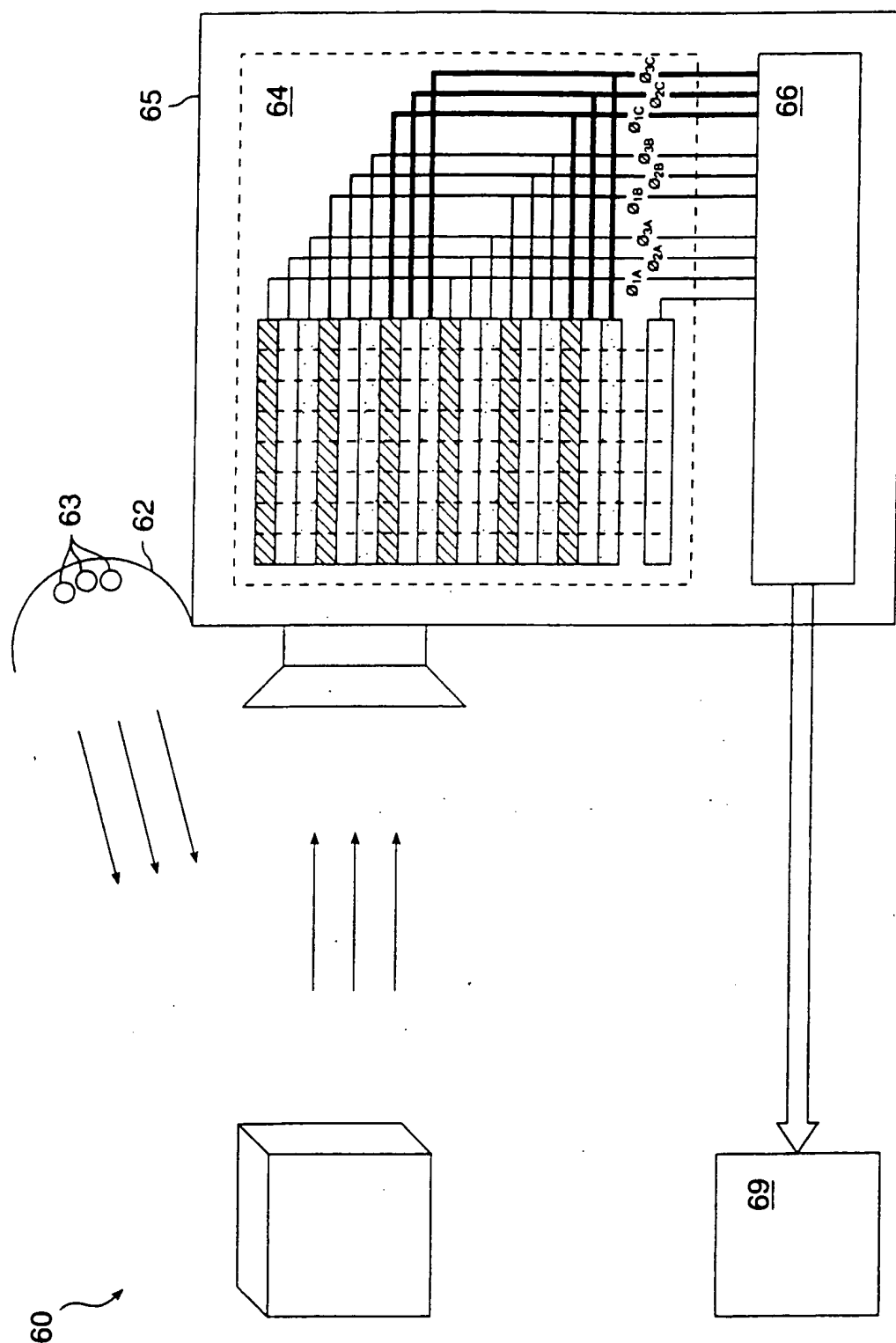


FIG. 6A

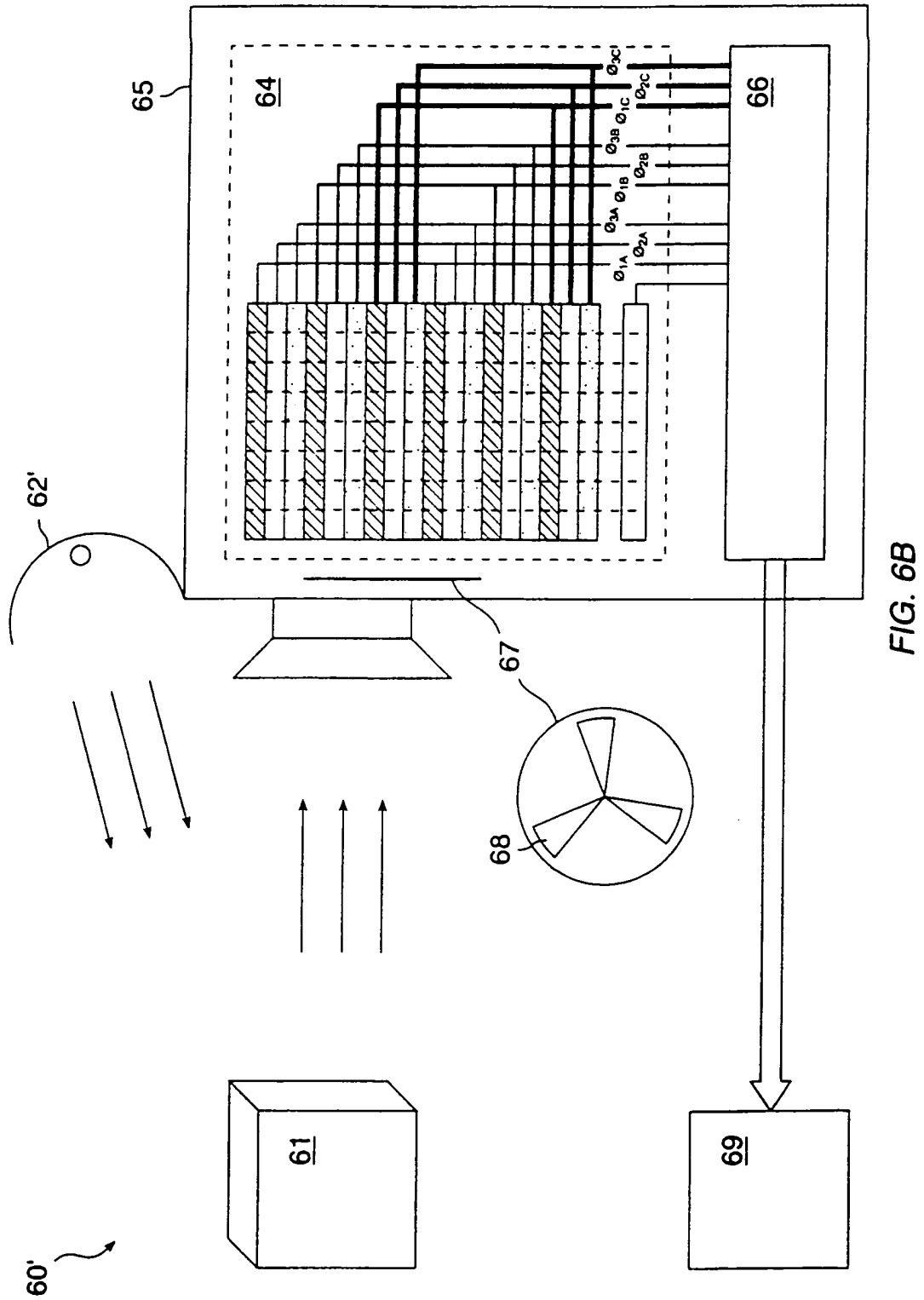


FIG. 6B

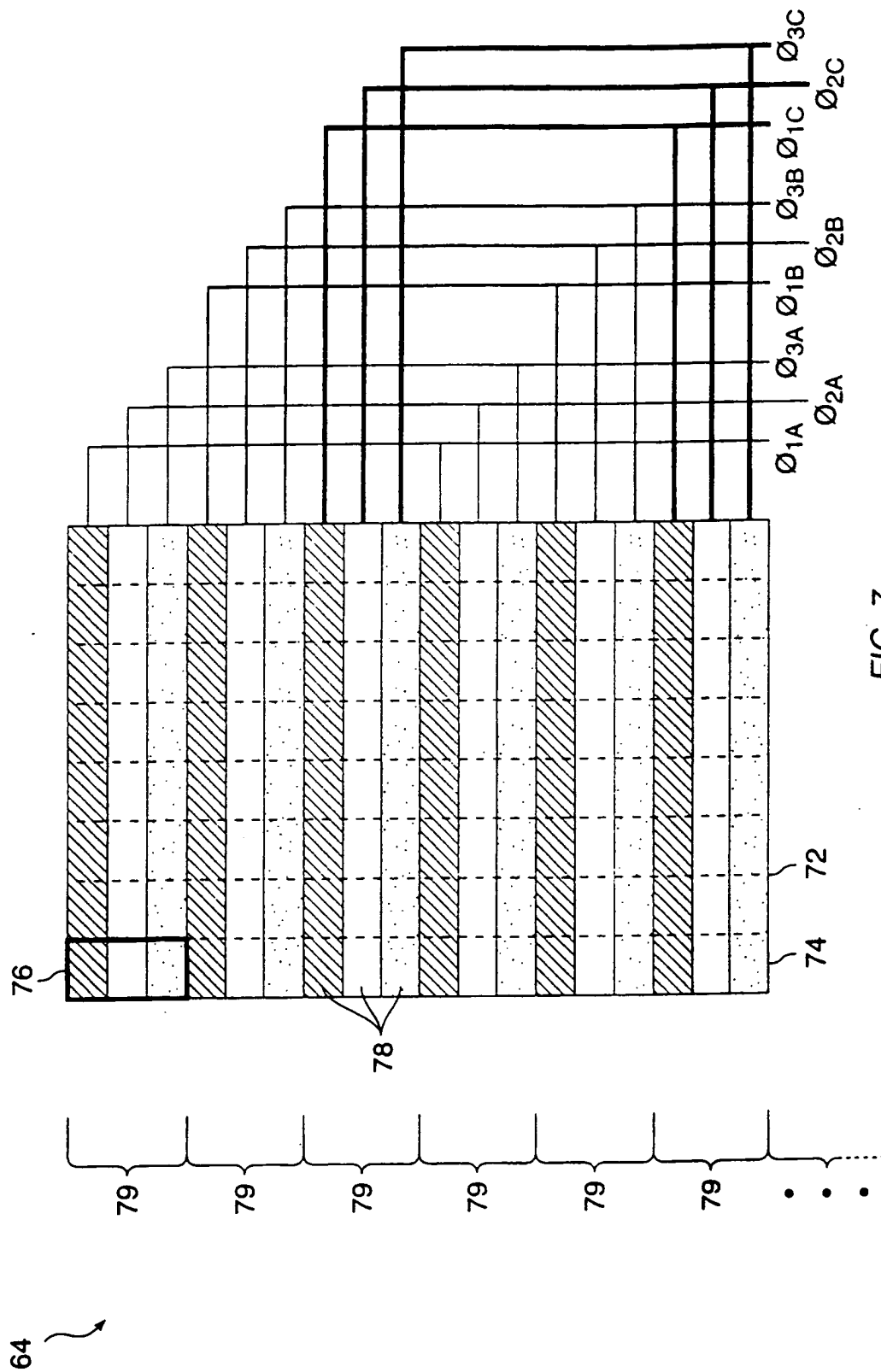


FIG. 7

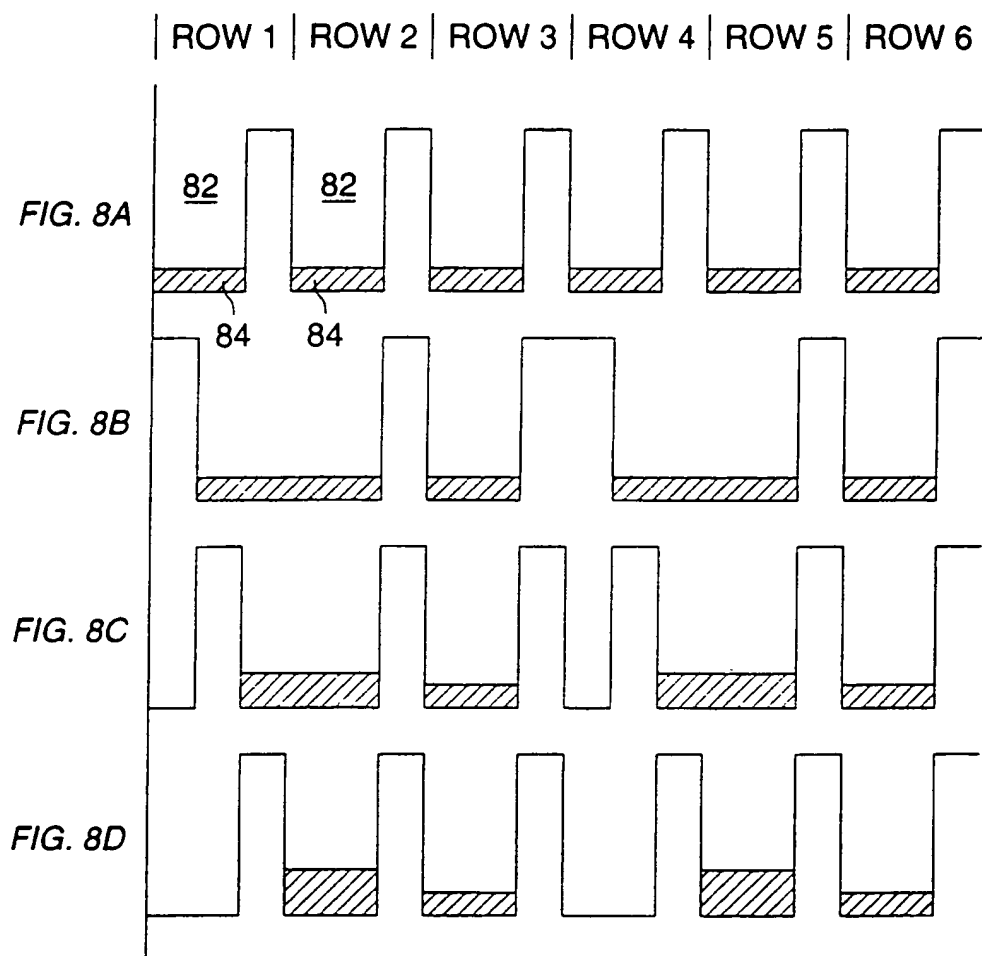


FIG. 8

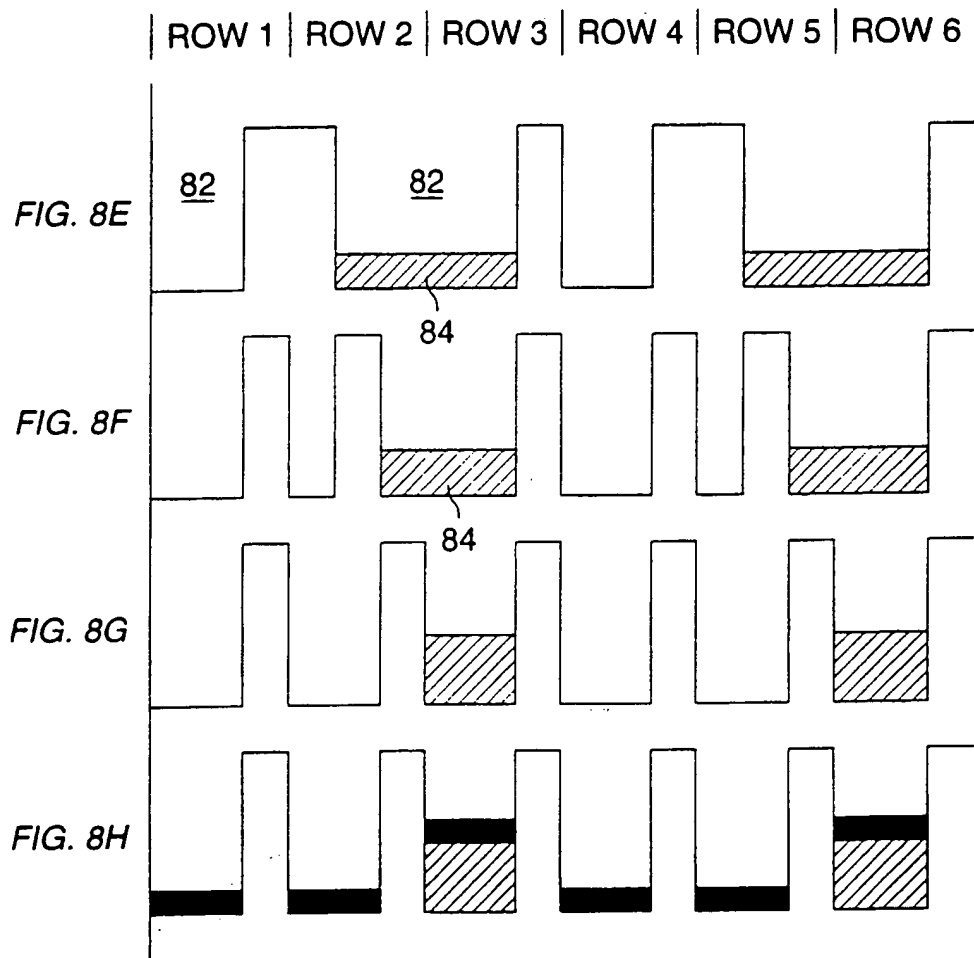


FIG. 8 (CONT.)

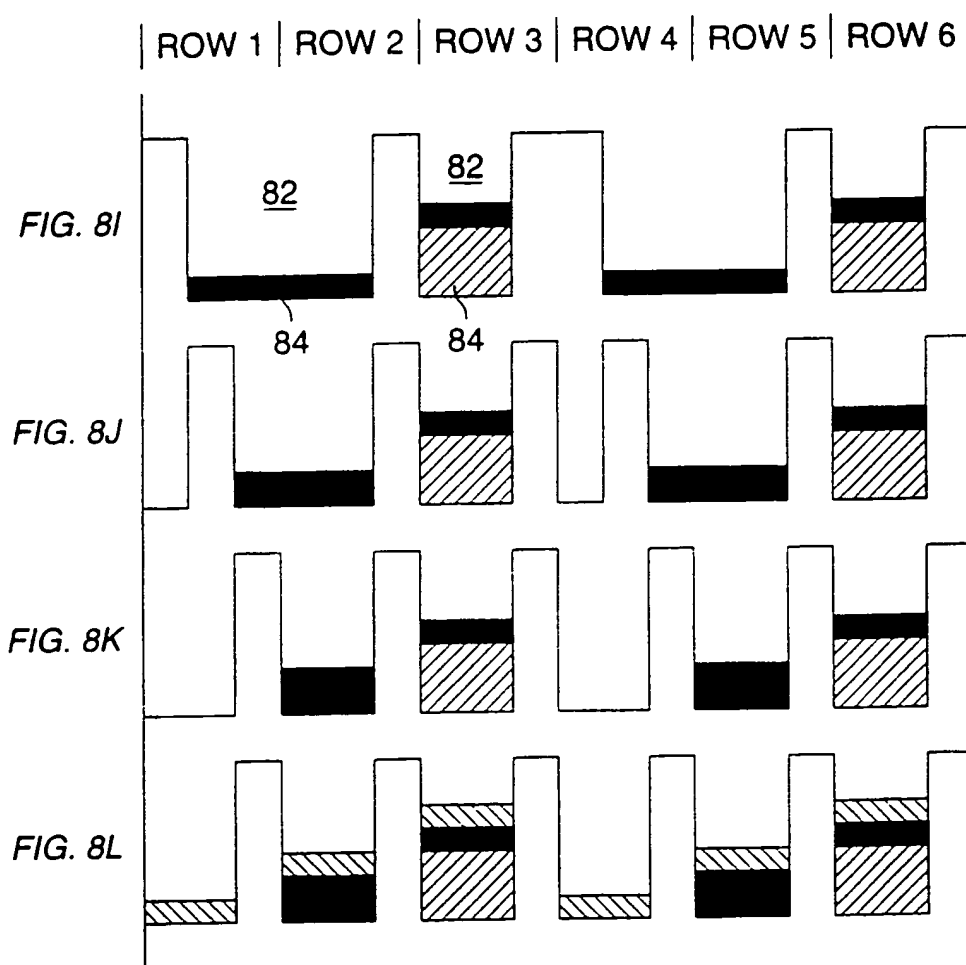


FIG. 8 (CONT.)

(19)



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(11)

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(71) Applicant: **LORAL FAIRCHILD CORPORATION**
Syosset, New York 11791 (US)

(72) Inventor: **Sayag, Michel**
Mountain View, California 94043 (US)

(74) Representative: **Grünecker, Kinkeldey,**
Stockmair & Schwanhäusser
Anwaltssozietät
D-80538 München (DE)

(54) **Electronic color snapshot technique and structure using very high resolution monochrome full frame CCD imagers**

(57) A technique and structure is used for producing high resolution color images using a monochrome area charge-coupled device (CCD) 64 and a sequential color illumination scheme. The monochrome CCD 64 comprises a plurality of semiconductor storage cells 76, the semiconductor storage cells 76 being configured in an array having vertical columns 74 and horizontal rows 79. The entire CCD 64 is exposed to a first color image. The charge packets 82 stored in two adjacent horizontal rows

as a result of the exposure are then shifted into a third horizontal row. The CCD 64 is then exposed to a second color image. The charge packets 82 stored in the first horizontal row as a result of the second exposure are then shifted into the second horizontal row. The CCD 64 is then exposed to a third and final color image. The CCD output is digitized and stored in a frame. The color information of a particular location on the CCD array 64 is derived by utilizing a simple set of equations.

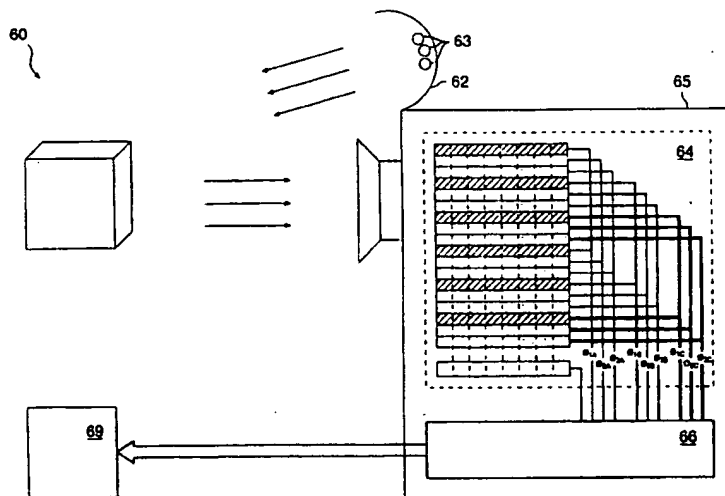


FIG. 6A

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European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 12 0751

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	US-A-5 101 266 (SCHLIG ET AL.)	1-11	H04N3/15
Y	* column 7, line 11 - column 11, line 41 *	12-14, 18-22	H04N9/04

Y	US-A-4 437 112 (TANAKA ET AL.)	12-14, 18-22	
	* column 4, line 54 - column 6, line 40 *		

A,P	EP-A-0 523 781 (N.V. PHILIPS' GLOEILAMPENFABRIKEN)	1-23	
	* column 5, line 12 - column 6, line 41 *		

A	US-A-4 760 441 (KOHNO)	1-23	
	* column 5, line 37 - column 6, line 48 *		

A	GB-A-2 063 617 (RCA CORPORATION)	1-23	
	* page 1, line 71 - page 3, line 121 *		

A	GB-A-2 161 671 (RCA CORPORATION)	1-23	
	* page 2, line 58 - page 5, line 33 *		

			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			H04N H01L
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 24 November 1995	Examiner Materne, A
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